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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,091	ARAYA ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated July 17, 2006. Claim 11 was amended. Claims 20-26 were added. Claims 11-26 of the application are pending. This office action is made non-final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 11-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996) in view of **Chang et al.** (U.S. Patent 6,269,467).

4.1 **Tammemae et al.** teaches AKKA: A tool for cosynthesis and prototyping. Specifically, as per claim 11, **Tammemae et al.** teaches a method in a LSI design and development process (Page 1, Para 1, L1-2; Page 1, Para 2, L2-5), for evaluating an architecture design for an algorithm design by performing a performance evaluation of at least one bus at a high-level stage of the design and development process (Page 1, Para 2, L2-4; Page 1, Para 4, L2; Page 2, Para 4, L3); the method comprising:

structuring source code describing the algorithm design in a general purpose high-level programming language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3), by isolating elements of the source code representing hardware units and software units (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

creating an evaluation function for counting data traffic that occurs on the at least one bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), the bus being a part of the source code realizing the data traffic between the elements representing hardware units and software units (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 1, Para 5, L5-6; Page 2, Para 2, L4);

modifying at least one element of the source code elements based on a result of an implementation of the evaluation function (Page 2, Para 5, L1-3; Page 2, Para 4, L3; Page 2, Para 2, L4);

performing the performance evaluation by simulating the modified source code elements and counting the data traffic on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Tammemae et al. does not expressly teach in response to the performance evaluation, modifying the configuration of the bus. **Chang et al.** teaches in response to the performance evaluation, modifying the configuration of the bus (CL27, L18-27; CL29, L29-35; CL33, L53-59). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Tammemae et al.** with the method of **Chang et al.** that included in response to the performance evaluation, modifying the configuration of the bus because that would allow the buses to be designed to meet the required system performance while minimizing the interface logic (CL27, L23-25); and selecting a high speed bus to handle high rate of data transfer and a low speed bus to handle a low data transfer rate (CL33, L53-59).

Per claim 12: **Tammemae et al.** teaches restructuring the source code based on the evaluated data traffic (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2); and

performing the performance evaluation again by simulating the restructured source code again (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1).

Per claim 13: **Tammemae et al.** teaches that a bus traffic is calculated from the evaluated data traffic with respect to the processing rate of the bus (Page 2, Para 5, L1-3).

Per claim 14: **Tammemae et al.** teaches feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by isolating in the source code new elements representing hardware units and new elements representing software units (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 15: **Tammemae et al.**. teaches that in response to the bus traffic, isolation of the source code into elements representing hardware units and elements representing software units is optimized (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 17: **Tammemae et al.** teaches that the variables loaded onto the bus consist of n bits while the bus consists of m bit lines, where n and m are both integers, and n is a multiple of m, and the bus traffic for the processing rate is produced such that the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate (Page 2, Para 5, L1-3). **Tammemae et al.** teaches that each variable access is counted using a counter and a log of the access of the variables is made. It is inherent that from the counting of the variable access to a bus, and the log of the variable accesses, it is possible to calculate the number of times the bus was used if the bus width was smaller than the variable length requiring multiple accesses to the bus for each variable loaded onto the bus.

Per claim 18: **Tammemae et al.** teaches that the general purpose high-level language is one of C language and C++ language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3).

Per claim 19: **Tammemae et al.** teaches that the evaluation function increments a counting value if a pre-defined variable is loaded onto the bus (Page 2, Para 5, L1).

5. Claims 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996) in view of **Chang et al.** (U.S. Patent 6,269,467), and further in view of **Raimi et al.** (U.S. Patent 5,604,895).

5.1 As per claim 16, **Tammemae et al.** and **Chang et al.** teach the method of claim 11. **Tammemae et al.** teaches creating the evaluation function (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4);

profiling the source code based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated (Page 2, Para 4, L3; Page 2, Para 2, L4);

structuring the source code into elements representing at least one of the hardware units and the software units for use in the architecture design by compiling the source code (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1);

calculating the data transfer rate on the bus by executing the compiled source code elements in a simulation program (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3);

calculating bus traffic with regard to a given processing rate of the bus (Page 2, Para 5, L1-3); and

performing evaluation of the performance of the bus in response to the bus traffic (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

Tammemae et al. and **Chang et al.** do not expressly teach after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated; upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written; and repeating the forgoing steps until the source code is completely read in up to a last line of source code. **Raimi et al.** teaches after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis (Abstract, L5-6; CL2, L20-22); determining whether the source code is to be modified based on whether a line of source code represents writing data to variables that are defined in advance and are loaded onto the bus to be evaluated (CL1, L26-32; CL1, L64-66; CL2, L37-54); upon determining that the source code is to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable is written (CL1, L26-32; CL1, L64-66; CL2, L23-29; CL2, L37-54); and repeating the forgoing steps until the source code is completely read in up to a last line of source code (Abstract, L5-6; CL2, L20-22). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Tammemae et al.** and **Chang et al.** with the method of **Raimi et al.** that included after creating the

evaluation function, sequentially reading in the source code line by line while effecting syntax analysis; determining whether the source code was to be modified based on whether a line of source code represented writing data to variables that were defined in advance and were loaded onto the bus to be evaluated; upon determining that the source code was to be modified, modifying the source code by embedding the evaluation function one of immediately before or immediately after the line of source code in which the variable was written; and repeating the forgoing steps until the source code was completely read in up to a last line of source code because that would allow generation of additional code to check for the occurrence of bus access events (CL1, L65-66).

5.2 As per claim 22, **Tammemae et al.** and **Raimi et al.** teach the method of claim 20. **Tammemae et al.** teaches that the bus configuration comprises the number of bit lines of the bus (Page 2, Para 5, L1-3); and isolation of the source code in hardware and software elements is optimized (Page 1, Para 2, L3; Page 1, Para 3, L7-8; Page 3, Fig. 1).

Tammemae et al. and **Raimi et al.** do not expressly teach in response to the bus traffic changing the number of bit lines of the bus. **Chang et al.** teaches in response to the bus traffic changing the number of bit lines of the bus (CL27, L18-27; CL29, L29-35; CL33, L53-59; CL39, L1-7).

6. Claims 20-21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tammemae et al.** ("AKKA: A tool for cosynthesis and prototyping", The Institution of Electrical Engineers, UK, 1996) in view of **Raimi et al.** (U.S. Patent 5,604,895).

6.1 As per claim 20, **Tammemae et al.** teaches a method in a LSI design and development process (Page 1, Para 1, L1-2; Page 1, Para 2, L2-5), for evaluating and facilitating an architectural design for an algorithm design by performing a performance evaluation of at least one bus at the architecture design being a high-level stage of the design and development process (Page 1, Para 2, L2-4; Page 1, Para 4, L2; Page 2, Para 4, L3); the method comprises the steps of:

structuring source code describing the algorithm design in a general purpose high-level programming language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3), by isolating the source code in hardware and software elements interconnected by the bus having a given bus configuration (Page 1, Para 2, L3-4; Page 1, Para 3, L7-8; Page 1, Para 4, L2; Page 1, Para 5, L5-6; Page 3, Fig. 1);

creating an evaluation function for evaluating data transfer that occurs on the bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), wherein the evaluation function counts and represents a number of times the source code effecting the data transfer on the bus (Page 2, Para 5, L1);

simulating the modified source code elements at the architecture design level and evaluating the data transfer on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3);

compiling the structured source code elements (Page 1, Para 4, L1-2);

executing the compiled source code elements on a simulation platform (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3);

calculating the bus traffic based on the number of times in effecting of data transfers according to the evaluation function and a given processing rate that is already known (Page 2, Para 5, L1-3);

performing the evaluation of the performance of the bus in response to the bus traffic being produced (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3); and

wherein the method is carried out again in response to the performance evaluation if necessary by starting with changing the bus configuration and restructuring the source code (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1).

Tammemae et al. and **Chang et al.** do not expressly teach sequentially reading in the source code; determining whether a line of source code represents writing data onto the bus to be evaluated; upon the determination, modifying the source code by embedding the evaluation function just before or after the line of source code in which the variable is written; and repeating the forgoing steps until the source code is completely read in and modified up to a last line of source code. **Raimi et al.** teaches sequentially reading in the source code (Abstract, L5-6; CL2, L20-22); determining whether a line of source code represents writing data onto the bus to be evaluated (CL1, L26-32; CL1, L64-66; CL2, L37-54); upon the determination, modifying the source code by embedding the evaluation function just before or after the line of source code in which the variable is written (CL1, L26-32; CL1, L64-66; CL2, L23-29; CL2, L37-54); and

repeating the forgoing steps until the source code is completely read in and modified up to a last line of source code (Abstract, L5-6; CL2, L20-22).

Per claim 21: **Tammemae et al.** teaches feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design at a high-level design stage by re-isolating the source code in hardware and software elements (Page 1, Para 2, L3-4; Page 1, Para 4, L1-2; Page 2, Para 5, L1-3).

Per claim 23: **Tammemae et al.** and **Chang et al.** do not expressly teach after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis. **Raimi et al.** teaches after creating the evaluation function, sequentially reading in the source code line by line while effecting syntax analysis (Abstract, L5-6; CL2, L20-22).

Per claim 24: **Tammemae et al.** teaches that the variables loaded onto the bus consist of n bits while the bus consists of m bit lines, where n and m are both integers, and n >= m, and the bus traffic for the processing rate is produced such that the number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate (Page 2, Para 5, L1-3). **Tammemae et al.** teaches that each variable access is counted using a counter and a log of the access of the variables is made. It is inherent that from the counting of the variable access to a bus, and the log of the variable accesses, it is possible to calculate the number of times the bus was used if the bus width was smaller than the variable length requiring multiple accesses to the bus for each variable loaded onto the bus.

Per claim 25: **Tammemae et al.** teaches that the general purpose high-level language is one of C language and C++ language (Page 1, Para 2, L2-3; Page 1, Para 3, L1-3).

Per claim 26: **Tammemae et al.** teaches that the evaluation function is to increment a counting value if a pre-defined variable is loaded onto the bus (Page 2, Para 5, L1).

Response to Arguments

7. Applicants' arguments with respect to 35 USC 112 first Paragraph, 35 USC 102 (a) and (b) and 35 USC 103 (a) rejections filed on July 17, 2006 have been considered. Claim rejections under 35 USC 112 first Paragraph are withdrawn in response to Applicants' arguments. Applicants' arguments with respect to 35 USC 102 (a) and (b) and 35 USC 103 (a) rejections are not persuasive. In addition, Applicants' amendment to claim 11 has necessitated using 103 (a) rejections for those claims which were previously rejected using 102 (a) and (b) rejections.

7.1 As per the applicants' argument that "Tammemae does not teach or suggest modifying the bus at the simulation stage; Tammemae does not teach or suggest the limitation of "in response to said performance evaluation, modifying the configuration of said bus", the Examiner has used a new reference **Chang et al.** in response to the Applicants' amendment to the claims.

Chang et al. teaches in response to the performance evaluation, modifying the configuration of the bus (CL27, L18-27; CL29, L29-35; CL33, L53-59).

7.2 As per the applicants' argument that "Raimi does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11; Raimi teaches that isolation between hardware and software elements are defined by "known" parameters; Adams does not overcome the shortcomings of the Tammemae reference; Adams teaches sequential reading of lines of source code for syntax analysis; Adams does not teach or suggest a software bus between the hardware and software elements of the simulation to exchange data traffic as required by claim 11", the Examiner takes the position that Tammemae teaches software modeling of the hardware and software elements of design for hardware/software co-simulation; the data transfer between the hardware elements and the software elements is modeled as part of the interface between the two; the bus in the software model is a software bus.

Tammemae teaches creating an evaluation function for counting data traffic that occurs on the at least one bus (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 2, Para 4, L3; Page 3, Fig. 1; Page 2, Para 2, L4), the bus being a part of the source code realizing the data traffic between the elements representing hardware units and software units (Page 1, Para 4, L2; Page 1, Para 2, L3-4; Page 1, Para 5, L5-6; Page 2, Para 2, L4);

modifying at least one element of the source code elements based on a result of an implementation of the evaluation function (Page 2, Para 5, L1-3; Page 2, Para 4, L3; Page 2, Para 2, L4); and

performing the performance evaluation by simulating the modified source code elements and counting the data traffic on the bus (Page 2, Para 5, L1-3; Page 3, Fig. 1; Page 4, Para 1, L2-3).

7.3 As per the applicants' argument that "a combination of Tammemae, Raimi and Adams does not teach or suggest every claimed feature of the invention; a prima facie case of obviousness has not been set forth", the Examiner respectfully disagrees. The Examiner has shown that all claimed features of the claims are taught by the prior art of **Tammemae et al., Chang et al.** and **Raimi et al.** The motivation for combing the art is also presented in the rejections of independent claims.

7.3 As per the applicants' argument that "Tammemae does not teach or suggest modifying the bus at the simulation stage; Tammemae does not teach or suggest the limitation of "determining whether a line of source code represents writing data onto the bus to be evaluated."", the Examiner takes the position that **Chang et al.** teaches modifying the bus at the simulation stage (CL27, L18-27; CL29, L29-35; CL33, L53-59). **Raimi et al.** teaches determining whether a line of source code represents writing data onto the bus to be evaluated (CL1, L26-32; CL1, L64-66; CL2, L37-54).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
August 3, 2006